Abstract

The interleaved clock generator generates *N* interleaved clock signals in response to an input clock signal. The interleaved clock generator comprises an interleaved clock generator of a first type for receiving the input clock signal and for generating *M* interleaved intermediate clock signals in response to the input clock signal. The interleaved clock generator of the first type includes either a multi-stage serial-delay circuit or a ring counter circuit. The interleaved clock generator additionally comprises *M* interleaved clock generators of a second type, each of which is each for receiving a respective one of the intermediate clock signals from the clock generator of the first type and for generating N/M of the *N* interleaved clock signals in response to the respective one of the intermediate clock signals. Each of the interleaved clock generators of the second type includes either a ring counter circuit or a multi-stage serial-delay circuit: a ring counter when the interleaved clock generator of the first type includes a multi-stage serial-delay circuit; a multi-stage serial-delay circuit when the interleaved clock generator of the first type includes a ring counter circuit.